

FIG. 1

FIG. 16.2 is a schematic diagram of a memory array structure in accordance with the present invention. The array is organized into rows and columns. Each row is connected to a word line (WL) and each column is connected to a bit line (BL). The array is controlled by a read/write circuit (155) and an address circuit (110). The read/write circuit is connected to the bit lines and the address circuit is connected to the word lines. The array is also connected to a group global mask (126) and a comparand register (180). The array is controlled by a bus (BUS) and a mask (MASK).

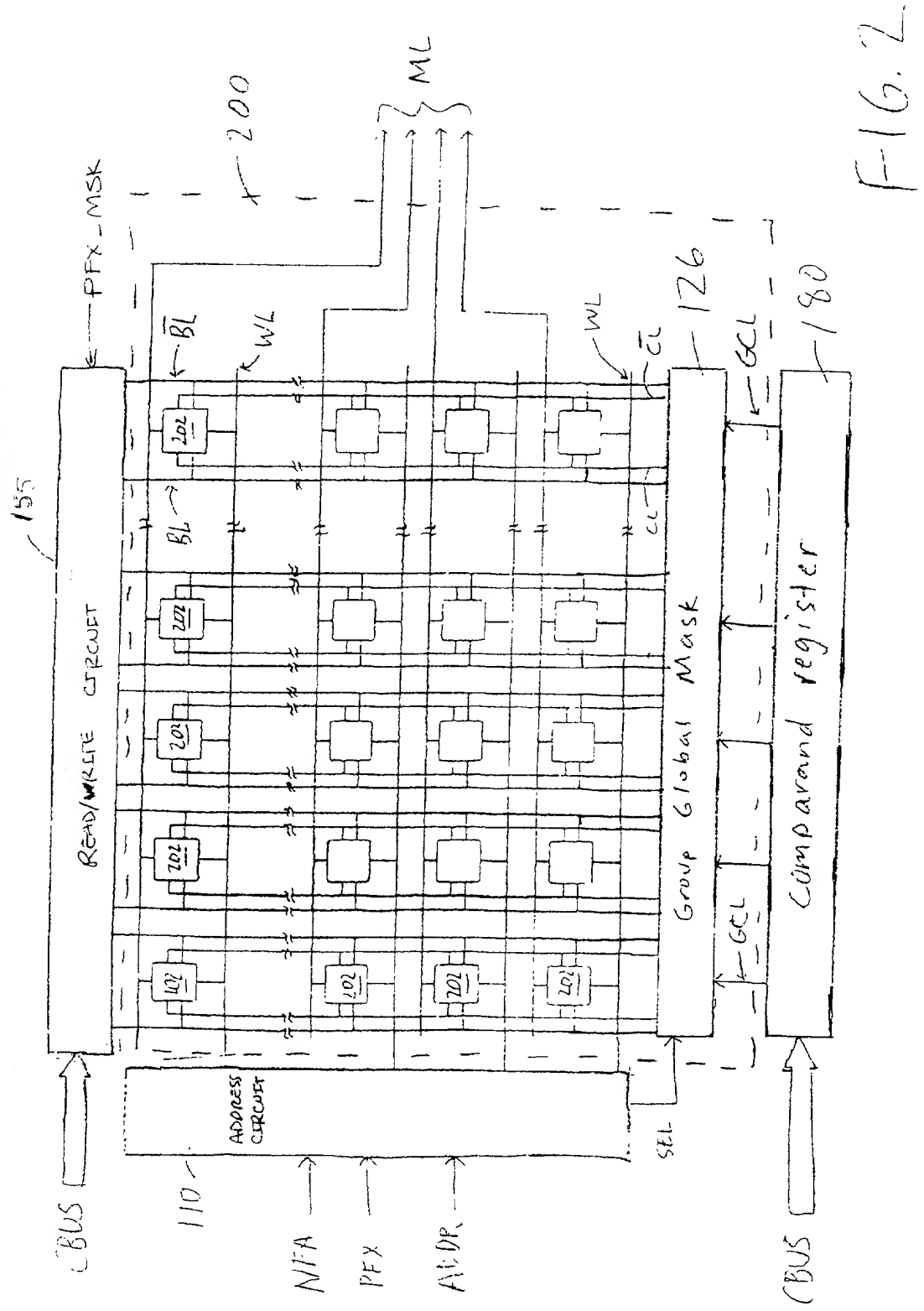


FIG. 16.2

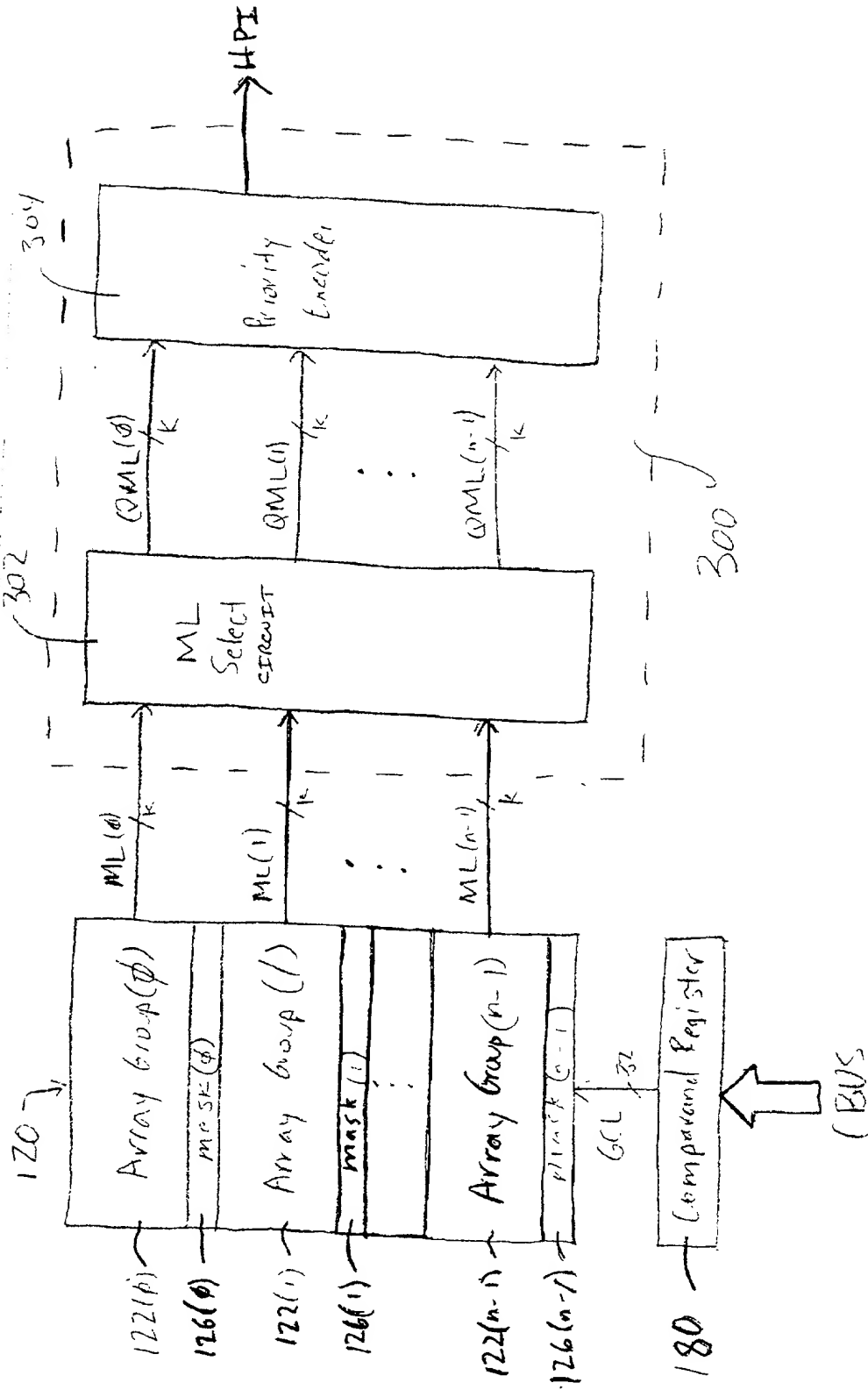


FIG. 16

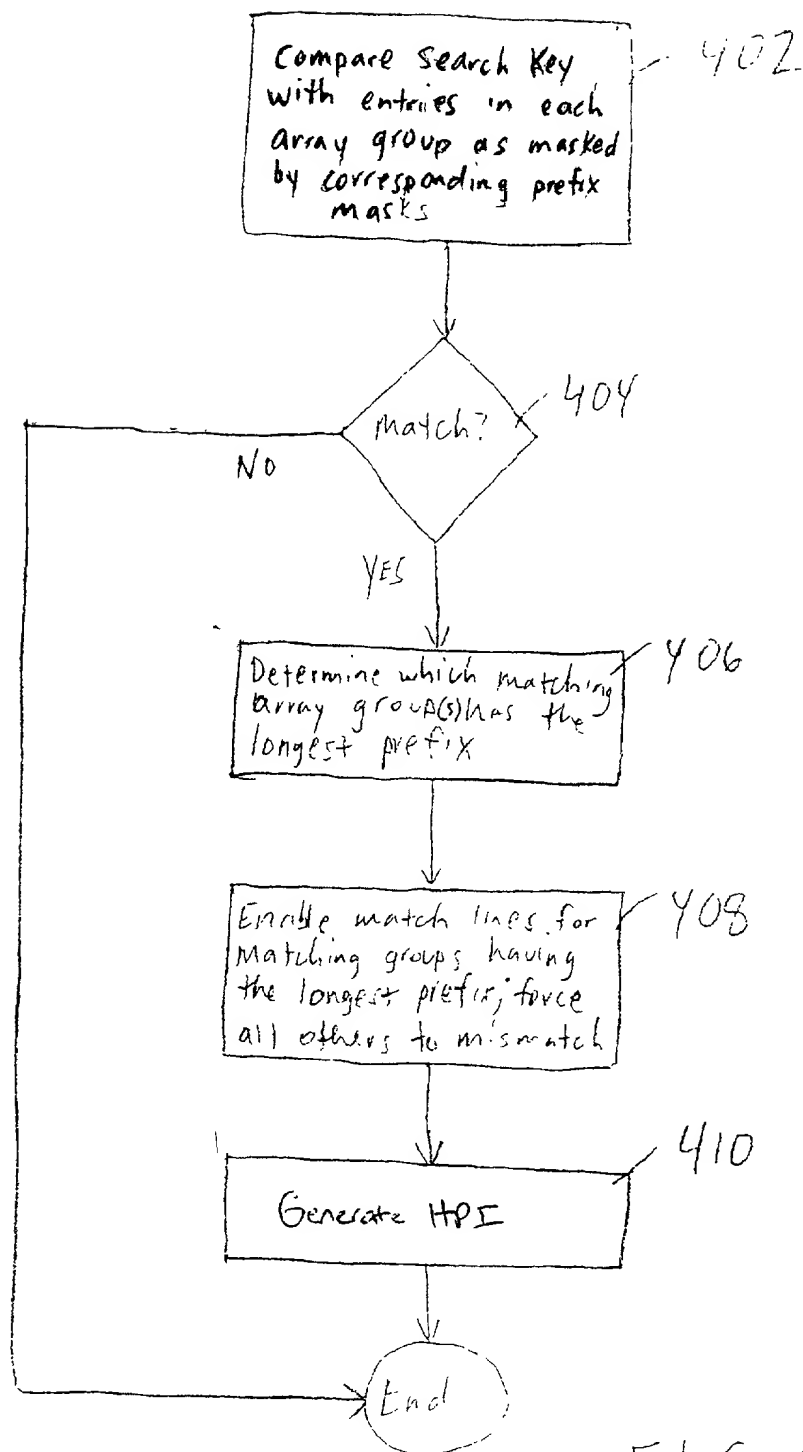


FIG 4

FIG. 5A

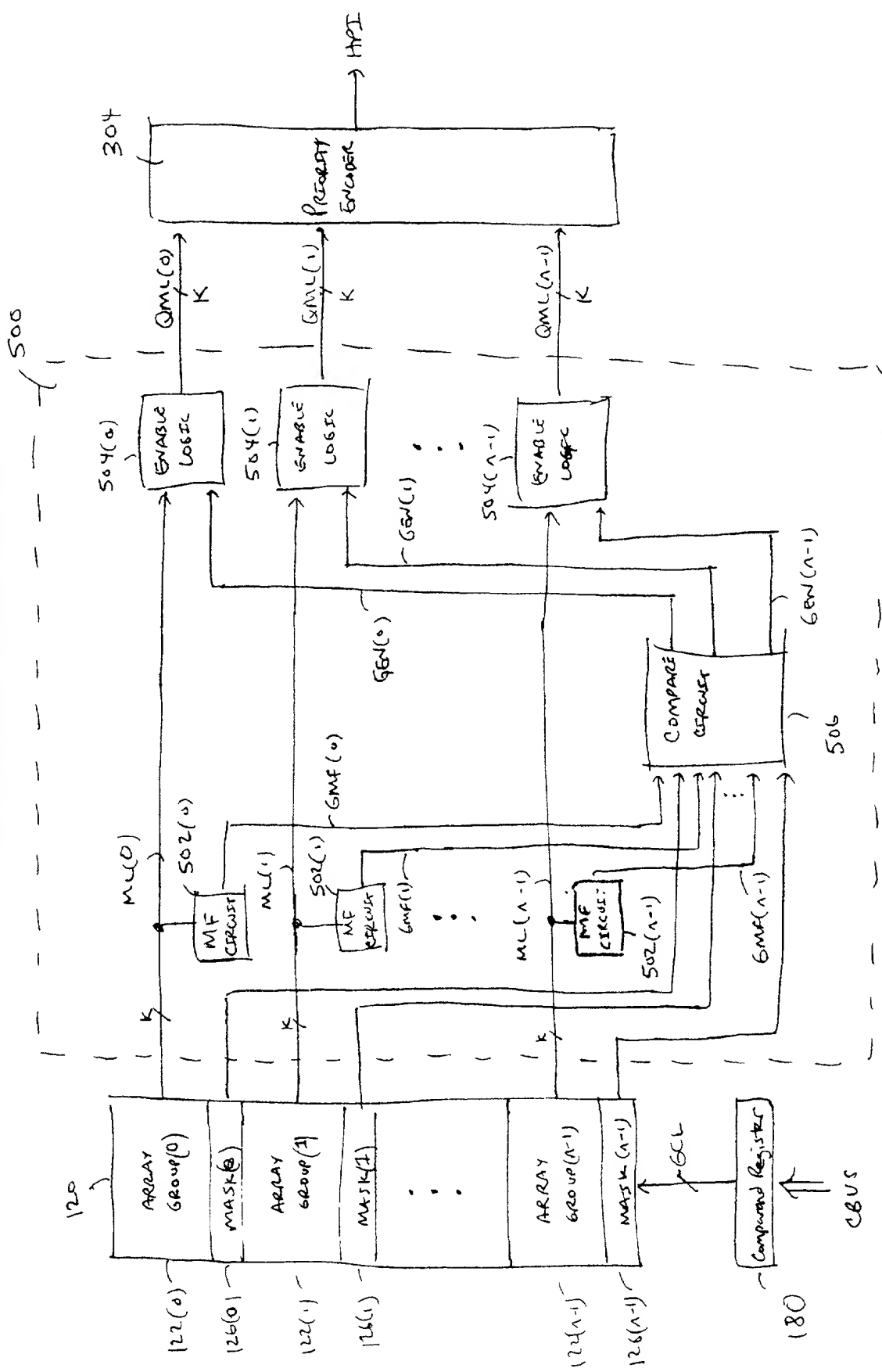
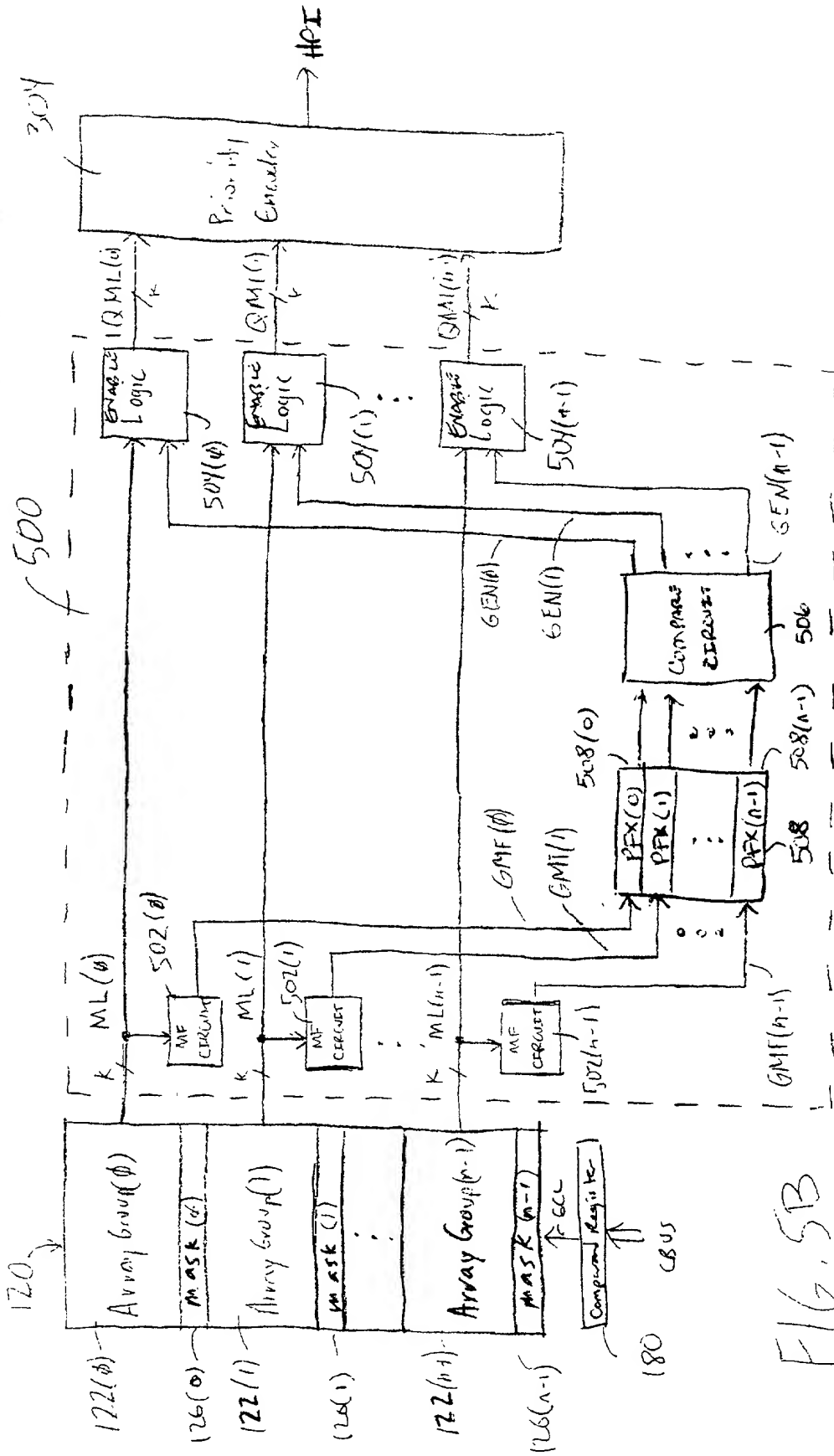


FIG. 5A



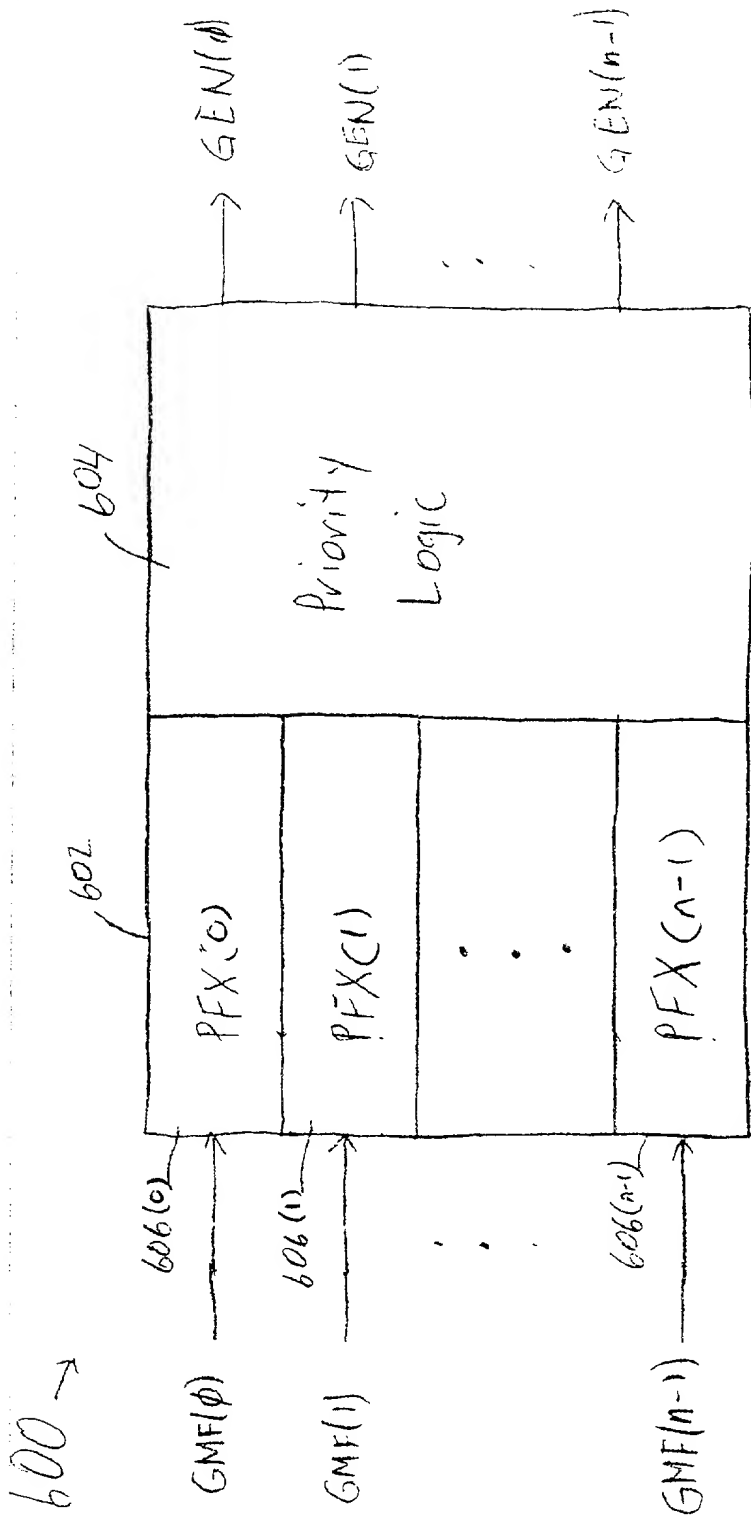


FIG. 6





112 →

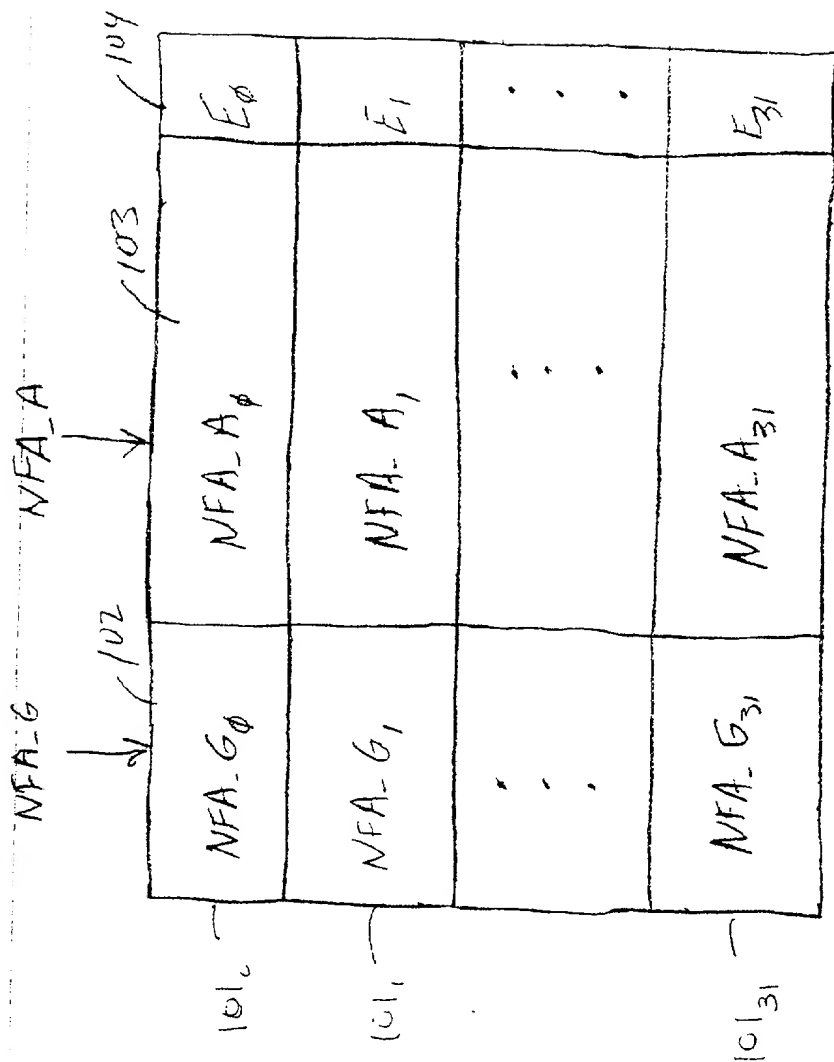


FIG. 8

FIG. 9 is a flowchart illustrating a process for updating an NFA table. The process begins with providing data and instructions to a CAM device 100 (902). This is followed by decoding the PFX to select in the NFA table 112 (904). A decision is made on whether the E bit is asserted (905). If the E bit is not asserted (No), the process proceeds to assign a new array group to the PFX (906), assert the E bit to logic 1 (908), store the PFX\_MSK in the mask and assert the MV bit to 1 (910), write data to the array @ NFA (912), compute a new NFA for the PFX (914), and update the NFA table (918), leading to the END state. If the E bit is asserted (Yes), the process proceeds to select a row using the NFA (920), write data to the array @ NFA (922), and generate a new NFA (923). A decision is made on whether the group is full (924). If the group is full (Yes), the process proceeds to compute a new NFA (930), update the NFA table (932), write the PFX\_MSK to the group global mask (934), assert the MV bit to 0 (936), and leads to the END state. If the group is not full (No), the process proceeds to update the NFA table (928) and leads to the END state.

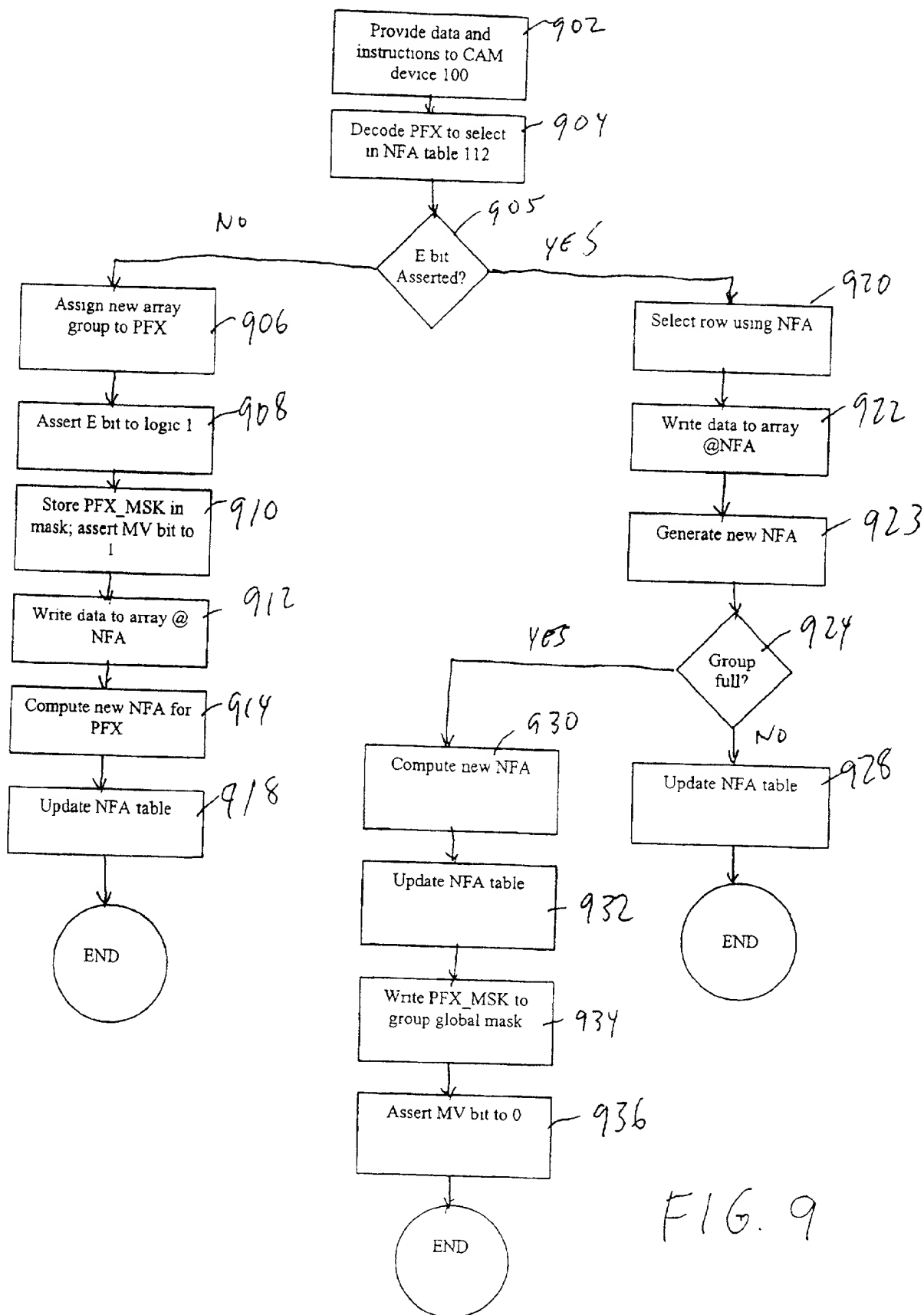


FIG. 9

